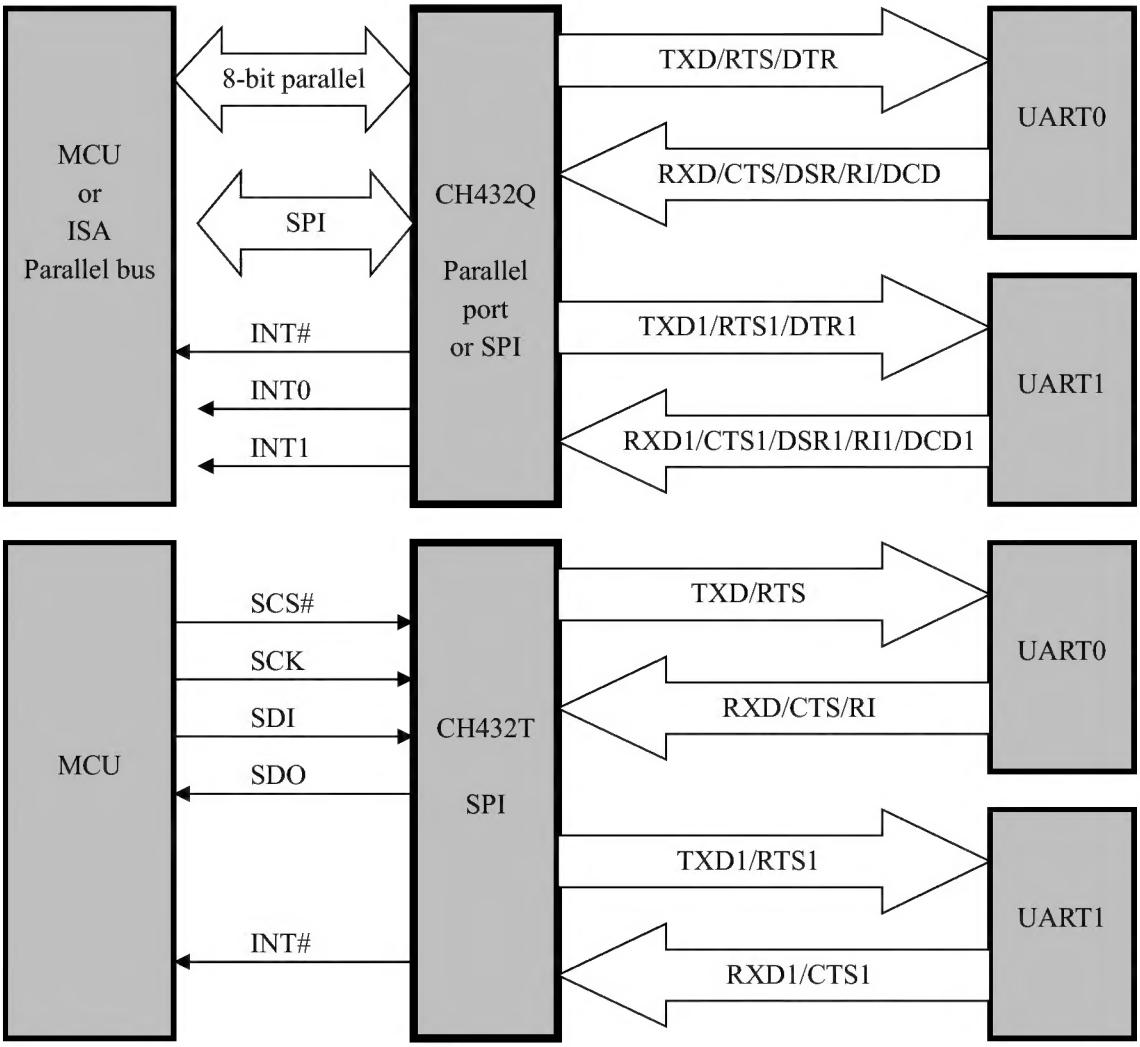
Dual UART Chip CH432

Datasheet
Version: 1A
http://wch.cn

1. Overview

CH432 is a dual-UART chip, which includes two UARTs compatible with 16C550, supports half-duplex automatic transceiver switching and IrDA infrared coding and decoding, and supports up to 4Mbps baud rate. It can be used for RS232 serial port extension of MCU/embedded system, high-speed serial port with automatic hardware rate control, RS485 communication, IrDA communication, etc. The figure below shows its general application block diagram.



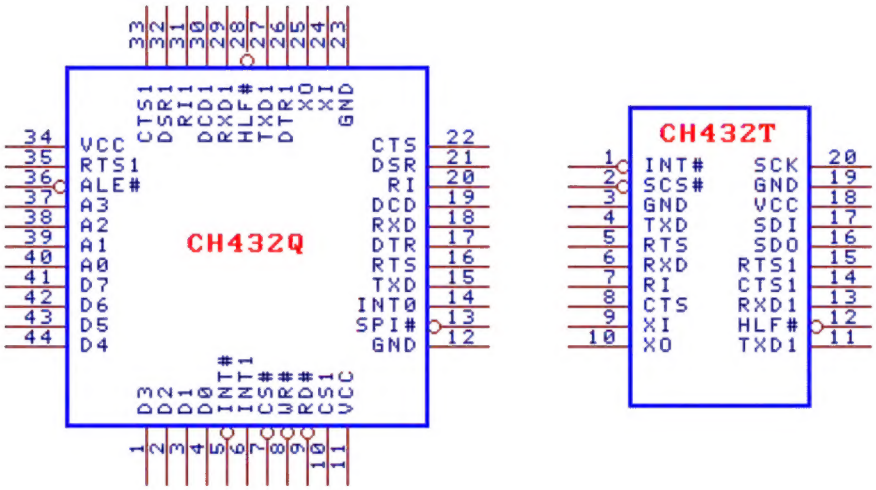
2. Features

- Two fully independent UARTs, compatible with 16C450, 16C550 and 16C552, and enhanced.
- 5/6/7/8 data bits, 1/2 stop bits.
- Support odd, even, mark, space, no parity.
- Programmable communication baud rate. Support communication baud rate of 115200bps and up to 4Mbps.
- Built-in 16-byte FIFO buffer, support four FIFO trigger levels.
- MODEM signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 level by

75232 chip.

- Automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Serial port frame error detection and Break line interval detection.
- Full-duplex and half-duplex serial communication, provide RTS serial port to send status signal and support RS485 transceiving automatic switch.
- Built-in SIR infrared Codec, 2,400bps to 115,200bps baud rate for IrDA infrared communication.
- Built-in clock oscillator, 0.92MHz to 32MHz crystal, 22.118MHz crystal by default.
- Two MCU interfaces are optional: 8-bit passive parallel interface at the speed of 10MB and SPI serial interface at the speed of 3MB/24MHz.
- The parallel interface contains an 8-bit data bus, a 4-bit address, and a 3-wire control: chip select input, write strobe and optional read strobe.
- The SPI serial interface includes SPI chip select, serial clock, serial input and output, and SPI output and input can be connected in parallel.
- The interrupt output pin is an optional connection and is active at low level. It can be replaced by querying the interrupt flag bit in the register.
- 5V or 3.3V supply voltage, serial port low-power sleep mode.
- QFP-44 and SSOP-20 lead-free packages, compatible with RoHS.

3. Package


CH432Q
VCC RTS1 ALE# A3 A2 A1 A0 D7 D6 D5 D4
CTS DSR RI DCD RXD DTR RTS TXD INT0 SPI# GND
CTS1 DSR1 RI1 DCD1 RXD1 HLF# TXD1 DTR1 XO XI GND
D3 D2 D1 D0 INT# INT1 CS## WR## RD## CS1 VCC
CH432T
INT# SCS# GND TXD RTS RXD RI CTS XI XO
SCK GND VCC SDI SDO RTS1 CTS1 RXD1 HLF# TXD1

Package	Body size		Lead pitch		Description	Part No.
QFP-44	10*10mm		0.8mm	31.5mil	Standard QFP 44-pin patch	CH432Q
SSOP-20	5.30mm	209mil	0.65mm	25mil	Shrink small outline 20-pin patch	CH432T

4. Pins

4.1. General description

CH432T in SSOP-20 package is a simplified version of CH432Q in QFP44 package. The pins with the same name have the same functions. In the following tables, the pin numbers listed directly apply to QFP-44 package, and the pin numbers in the brackets apply to SSOP20 package, and those marked in gray are redefinition for the pins with dual functions.

4.2. Power supply and system signal line

Pin No.	Pin Name	Pin Type	Description
11,34 (18)	VCC	Power	Positive power supply
12,23 (3,19)	GND	Power	Common ground
24 (9)	XI	Input	Input of the crystal oscillator, requires an external crystal and oscillation capacitor
25 (10)	XO	Output	Reverse-phase output of the crystal oscillator, requires an external crystal and oscillation capacitor
28 (12)	HLF#	Input	Half-duplex communication mode enabled, active low, built-in weak pull-up resistor

4.3. Local interface signal line

Pin No.	Pin Name	Pin Type	Description
13	SPI#	Input	Selection of interface mode: Parallel port mode at high level, SPI mode at low level
36	ALE#	Input	Selection of parallel address mode: Direct address mode at high level, multiplexed address mode at low level
1-4, 41-44	D7～D0	Three-status output and input	Bidirectional data signal line in parallel mode Address and data multiplexing signal line in parallel multiplexed address mode
1 (20)	SCK	Input	SPI serial clock input in SPI mode
42 (17)	SDI	Input	SPI serial data input in SPI mode
41 (16)	SDO	Three-status output	SPI serial data output in SPI mode
37-40	A3～A0	Input	Address line input in parallel direct address mode
37	ALE	Input	Address latch enabling input in parallel multiplexed address mode, active high
9	RD#	Input	Read strobe input in parallel port mode, active low
8	WR#	Input	Write strobe input in parallel port mode, active low
7	CS#	Input	Chip select control input in parallel port mode, active low
7 (2)	SCS#	Input	SPI chip select input in SPI port mode, active low
10	CS1	Input	Chip select control input in parallel port mode, active high
5 (1)	INT#	Open-drain output	Interrupt request signal output, active low
14	INT0	Three-status output	UART0 interrupt request output, active high, built-in weak pull-up resistor
6	INT1	Three-status output	UART1 interrupt request output, active high, built-in weak pull-up resistor

4.4. UART0 signal line

Pin No.	Pin Name	Pin Type	Description
22 (8)	CTS	Input	MODEM signal, clear to send, active low, built-in weak pull-up resistor
21	DSR	Input	MODEM signal, data device ready, active low, built-in weak pull-up resistor

20 (7)	RI	Input	MODEM signal, ring indicator, active low, built-in weak pull-up resistor
19	DCD	Input	MODEM signal, carrier detect, active low, built-in weak pull-up resistor
18 (6)	RXD	Input	Asynchronous serial data input, built-in weak pull-up resistor
17	DTR	Output	MODEM signal, data terminal ready, active low
16 (5)	RTS	Output	MODEM signal, request to send, active low Serial data sending status indication during half-duplex communication, active high
15 (4)	TXD	Output	Asynchronous serial data output

4.5. UART1 signal line

Pin No.	Pin Name	Pin Type	Description
33 (14)	CTS1	Input	MODEM signal, clear to send, active low, built-in weak pull-up resistor
32	DSR1	Input	MODEM signal, data device ready, active low, built-in weak pull-up resistor
31	RI1	Input	MODEM signal, ring indicator, active low, built-in weak pull-up resistor
30	DCD1	Input	MODEM signal, carrier detect, active low, built-in weak pull-up resistor
29 (13)	RXD1	Input	Asynchronous serial data input, built-in weak pull-up resistor
26	DTR1	Output	MODEM signal, data terminal ready, active low
35 (15)	RTS1	Output	MODEM signal, request to send, active low Serial data sending status indication during half-duplex communication, active high
27 (11)	TXD1	Output	Asynchronous serial data output

5. Configuration

5.1. Half-duplex configuration

UARTs of CH432 support full-duplex and half-duplex communication. When HLF# pin is grounded or connected to low level, CH432 will work in the half-duplex communication mode. This type of half-duplex communication can be divided into two specific applications: half-duplex serial port (including but not limited to RS485 communication application) and IrDA infrared serial port SIR. In a half-duplex serial port application, RTS pin (RTS1 pin for UART1) is used to indicate the status of serial data being sent. It is active high and can be used to automatically control the transceiver switching of RS485. In the infrared serial port SIR application, RXD and TXD pins can be directly connected to RXD and TXD pins of infrared transceivers such as ZHX1810, HSDL3000, TFBS4711 and TFDU4100. CH432 automatically realizes infrared encoding and decoding. The table below shows the half-duplex configuration of UARTs.

Pin combination status	HLF# pin is suspended or connected to high level	HLF# pin is grounded or connected to low level
CTS pin is connected to high level	UART0 is full-duplex communication	UART0 is the infrared serial port SIR
CTS pin is grounded or connected to low level	CTS is used for MODEM signal	UART0 is half-duplex communication, e.g., RS485

CS1 pin is connected to high level	UART1 is full-duplex communication CTS1 is used for MODEM signal	UART1 is full-duplex communication
CTS1 pin is grounded or connected to low level		UART1 is half-duplex communication, e.g., RS485

5.2. Internal clock

CH432 has an internal clock oscillator. The external clock signal required by UART can be generated only by connecting a crystal between XI and XO pins and connecting the oscillating capacitor for XI and XO pins to ground respectively. If the crystal and the capacitor are not connected, CH432 can also directly input the clock from the external clock source through XI pin.

CK2X is the bit 5 of IER register for UART1. The internal CK2X of CH432 selects the external clock signal of XI pin to perform 1/12 frequency division or frequency doubling, and the generated internal reference clock is provided to two UARTs. CK2X is 0 by default. If CK2X is 0, 1/12 frequency division is selected. If CK2X is 1, frequency doubling is selected. If it is required to be compatible with the existing 16C550 serial port chips, the internal clock frequency shall be 1.8432MHz and the corresponding maximum baud rate shall be 115200bps, so the default external clock frequency is 22.118MHz. If a high baud rate is required, set CK2X to 1 and select a high external clock frequency. If a baud rate with a special value is required, an external clock or crystal with a specific frequency shall be selected.

The following table shows the internal clock frequency and maximum baud rate generated for the UARTs according to CK2X value and external crystal frequency.

External input clock frequency or external crystal frequency	CK2X=0, internal 1/12 frequency division		CK2X=1, internal frequency doubling	
	Internal clock frequency	Maximum baud rate	Internal clock frequency	Maximum baud rate
32MHz			64MHz	4Mbps
22.1184MHz	1.8432MHz	115.2Kbps	44.2368MHz	2.7648Mbps
18.432MHz			36.864MHz	2.304Mbps
14.7456MHz			29.4912MHz	1.8432Mbps
11.0592MHz	0.9216MHz	57.6Kbps	22.1184MHz	1.3824Mbps
7.3728MHz	0.6144MHz	38.4Kbps	14.7456MHz	921.6Kbps
3.6864MHz	0.3072MHz	19.2Kbps	7.3728MHz	460.8Kbps
0.9216MHz			1.8432MHz	115.2Kbps

5.3. Local interface mode

CH432T only supports SPI synchronous serial interface on the local terminal, but CH432Q provides two interface modes on the local terminal: universal 8-bit passive parallel interface and SPI synchronous serial interface. During power on reset, CH432Q will sample the state of SPI# pin. If SPI# is at low level (grounded), SPI serial interface is selected; otherwise, the parallel interface is selected.

If the parallel interface is selected, CH432Q selects the address mode based on the state of ALE# pin: direct address and multiplexed address. If ALE# pin is at low level, the multiplexed address mode is selected; otherwise, the direct address mode is selected. In the direct address mode, the address is directly input from the pins A3-A0. In the multiplexed address mode, the address is controlled by ALE pin and input from the pins D3-D0 into the latch.

Pin state	ALE# pin is at high level	ALE# pin is at low level
SPI# pin is at high level	Direct address 8-bit parallel port mode	Multiplexed address 8-bit parallel port mode

SPI# pin is at low level	SPI serial interface mode

6. Registers

CH432 is compatible with the industrial standard 16550 and is enhanced. The bits marked in gray in the table are enhanced functions. For other registers, please refer to the description of the single-UART chip 16C550. In the register address space distribution, 8 registers starting from address 00H are the registers for UART0, and 8 registers starting from address 08H are the registers for UART1. The registers for UART0 and UART1 are the same except for the different starting addresses and SLP/CK2X register bit in the following table. In the table, DLAB is bit 7 of the LCR register, X means that the value of DLAB is not concerned, RO means the register is read-only, WO means the register is write-only, and R/W means the register is readable and writable.

Address	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RO	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WO	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	SLP/CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	0	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	0	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	0	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	△DCD	△RI	△DSR	△CTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table shows the default values of UART registers after power-on reset or UART soft reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Keep	Keep	Keep	Keep	Keep	Keep	Keep	Keep
FIFO	Reset, including the transmit FIFO and receive FIFO							
TSR	Reset; TSR is UART transmit shift register							
RSR	Reset; RSR is UART receive shift register							
Other	Not defined							

RBR: Receive buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this register. If FIFOEN is 1, the data received from the RSR register will be firstly stored in the receive FIFO, and then read out through the register.

THR: Transmit hold register, including the transmit FIFO, for writing the data to be transmitted. If FIFOEN is 1, the written data will be firstly stored in the transmit FIFO, and then output one by one through

the TSR register.

IER: Interrupt enable register, including enhanced function control bit and UART interrupt enable.

RESET: When this bit is set to 1, soft reset the UART, and this bit can be cleared automatically without software.

LOWPOWER: When this bit is 1, the internal reference clock of UART will be disabled, so that the UART will enter a low-power status.

SLP/CK2X: the purpose of UART0 at the bit is different from that of UART1, SLP for UART0. When the bit is 1, disable the clock oscillator, so that both UART0 and UART1 will sleep. CK2X for UART1. When the bit is 1, force the external clock signal for frequency doubling and then use it as the internal reference clock of UART0 and UART1.

IEMODEM: When this bit is 1, it will allow modem input status change interrupt.

IELINES: When this bit is 1, it will allow receive line status interrupt.

IETHRE: When this bit is 1, it will allow transmit hold register null interrupt.

IERECV: When this bit is 1, it will allow received data interrupt.

IIR: Interrupt recognition register, for analyzing the interrupt source and processing.

FIFOENS: This bit is the FIFO enabled status, and 1 means that the FIFO has been enabled.

IIR register bit				Precedence level	Interrupt Type	Interrupt sources	To clear interrupt
IID3	IID2	IID1	NOINT				
0	0	0	1	none	No interrupt generated	No interrupt	
0	1	1	0	1	Receive line status	OVERR, PARERR, FRAMEERR, BREAKINT	Read LSR
0	1	0	0	2	Receive data available	The number of bytes received reaches the trigger point of FIFO	Read RBR
1	1	0	0	2	Receive data timeout	No next data is received when the time of four data is exceeded	Read RBR
0	0	1	0	3	THR empty	Transmit hold register empty, IETHRE changes from 0 to 1 to re-enable the interrupt	Read IIR Or write THR
0	0	0	0	4	MODEM input change	△CTS, △DSR, △RI, △DCD	Read MSR

FCR: FIFO control register, used to enable and reset FIFO.

RECVTG1 and RECVTG0: Set the trigger point for receiving FIFO interrupt and hardware flow control. 00 corresponds to 1 byte, that is, interrupt available for receiving data is generated when a byte is received, and RTS pin is automatically invalid when hardware flow control is enabled. 01 corresponds to 4 bytes, 10 corresponds to 8 bytes, and 11 corresponds to 14 bytes.

TFIFORST: When this bit is set to 1, the data in the transmit FIFO (TSR not included) is cleared. This bit can be cleared automatically without software.

RFIFORST: When this bit is set to 1, the data in the receive FIFO (RSR not included) is cleared. This bit can be cleared automatically without software.

FIFOEN: When this bit is 1, FIFO is enabled. When this bit is cleared, FIFO is disabled. After FIFO is disabled, it is 16C450 compatible mode, it means only one byte in FIFO.

LCR: Line control register, used to control the format of UART communication.

DLAB: This bit is the access enable of the divisor latch. When it is 1, DLL and DLM can be accessed; when it is 0, RBR/THR/IER can be accessed.

BREAKEN: When this bit is 1, it is mandatory to generate a BREAK line interval.

PARMODE1 and PARMODE0: When PAREN is 1, set the format of the parity bit: 00 means odd parity,

01 means even parity, 10 means mark bit (MARK, set to 1), 11 means blank bit (SPACE, cleared).

PAREN: When this bit is 1, it is allowed to generate parity bit during transmission and check parity bit when receiving. If it is 0, there is no parity bit.

STOPBIT: When this bit is 1, two stop bits. When it is 0, one stop bit.

WORDSZ1 and WORDSZ0: Set the word length. 00 means 5 data bits, 01 means 6 data bits, 10 means 7 data bits, and 11 means 8 data bits.

MCR: Modem control register, used to control MODEM output.

AFE: When this bit is 1, the hardware automatic flow control of CTS and RTS is allowed. If AFE is 1, then UART will continuously send the next data only when it detects that the CTS pin input is valid (active low). Otherwise, UART transmission will be suspended, and the CTS input status change will not generate the MODEM status Interrupt when AFE is 1. If AFE is 1 and RTS is 1, UART will automatically validate the RTS pin (active low) when the receive FIFO is empty. UART will automatically invalidate the RTS pin when the number of received bytes reaches the trigger point of FIFO and will re-validate the RTS pin when the receive FIFO is empty. You can connect your own CTS pin to the other party's RTS pin through the hardware automatic band rate control, and can connect your own RTS pin to the other party's CTS pin.

LOOP: When this bit is 1, the test mode of the internal loop will be enabled. In the test mode of the internal loop, all external output pins of UART are at the invalid status, TXD internally returns to RXD (i.e., the output of TSR internally returns to the input of RSR), RTS internally returns to CTS, DTR internally returns to DSR, OUT1 internal returns to RI and OUT2 internally returns to DCD.

OUT2: If this bit is 1, the interrupt request output of UART is allowed. Otherwise, UART will not generate the actual interrupt request.

OUT1: This bit is a user-defined MODEM control bit, and no actual output pin is connected.

RTS: If this bit is 1, the RTS pin output is valid (active low). Otherwise, the RTS pin output is invalid.

DTR: If this bit is 1, the DTR pin output is valid (active low). Otherwise, the DTR pin output is invalid.

LSR: Line status register, used for querying and analyzing the status of UART.

RFIFOERR: When this bit is 1, there is at least one PARERR, FRAMEERR or BREAKINT error in the receive FIFO.

TEMT: When this bit is 1, the transmit hold register (THR) and the transmit shift register (TSR) are both empty.

THRE: When this bit is 1, the transmit hold register (THR) is empty.

BREAKINT: When this bit is 1, the BREAK line interval is detected.

FRAMEERR: When this bit is 1, the frame error of the data being read from the receive FIFO due to lack of a valid stop bit.

PARERR: When this bit is 1, the parity error of the data being read from the receive FIFO.

OVERR: When this bit is 1, the receive FIFO buffer area has overflowed.

DATARDY: When this bit is 1, there is received data in the receive FIFO. After reading all data in the FIFO, this bit will be automatically cleared.

MSR: Modem status register, used to query the MODEM status.

DCD: This bit is the reverse bit of the DCD pin. When it is 1, the DCD pin is valid (active low).

RI: This bit is the reverse bit of the RI pin. When it is 1, the RI pin is valid (active low).

DSR: This bit is the reverse bit of the DSR pin. When it is 1, the DSR pin is valid (active low).

CTS: This bit is the reverse bit of the CTS pin. When it is 1, the CTS pin is valid (active low).

△DCD: When this bit is 1, the DCD pin input status has changed.

△RI: When this bit is 1, the input status of the RI pin has changed.

△DSR: When this bit is 1, the input status of the DSR pin has changed.

△CTS: When this bit is 1, the input status of the CTS pin has changed.

SCR: user-defined register.

DLL and DLM: Baud rate divisor latch. DLL is the low byte and DLM is the high byte. The 16-bit divisor formed by the two is used for baud rate generator composed of a 16-bit counter. The divisor = UART internal reference clock / 16 / the required communication baud rate. If the internal reference clock of UART is 1.8432MHz and the required baud rate is 9600bps, then the divisor =1843200/16/9600=12.

7. Functional description

7.1. Query and interrupt

CH432 has three interrupt request output pins. INT0 pin is an interrupt request of UART0, its three-state output is controlled by OUT2 of MCR for UART0, and the output is allowed when OUT2 is 1. INT1 pin is an interrupt request of UART1, its three-state output is controlled by OUT2 of MCR for UART1, and the output is allowed when OUT2 is 1. INT# pin is an active low open-drain output pin, an external pull-up resistor may be required when the MCU is connected. It is "NOR" of INT0 and INT1 in logic function, and INT# pin outputs low level when INT0 or INT1 is valid (three-state output is allowed and high level is output), otherwise, INT# pin does not output.

If only INT# pin is connected, namely, two UARTs share an interrupt request, the MCU shall first analyze which UART has the interrupt request after going into the interrupt service program. After going into the interrupt service program, the MCU firstly reads the IIR register of UART0. If there is an interrupt, process and exit it. If there is no interrupt, read the IIR register of UART1. If there is an interrupt, process and exit it, and if there is no interrupt, exit it directly. After ensuring that it is an interrupt of a certain UART, further analyze the LSR register to analyze the cause of the interrupt and process it if necessary.

If INT0 and INT1 pins are connected, the MCU can directly know which UART has interrupt request, and the IIR register can be directly read, analyze and process the interrupt. When the three-state output is disabled (OUT2 of the MCR register is 0), the built-in weak pull-up resistor will make INT0 and INT1 output weak high level, and make their defaults to low level by externally connecting 10KΩ-100KΩ pull-down resistor.

If UART works in the interrupt mode, it is needed to set the IER register to allow the corresponding interrupt request, and set OUT2 in the MCR register to allow interrupt output.

If UART works in query mode, it is not required to set OUT2 of IER and MCR. Query the LSR register and analyze and process it.

7.2. UART operation

Transmit hold register (THR) empty interrupt sent by UART (the lower 4 bits of IIR are 02H) refers to the transmit FIFO empty. The interrupt is cleared after the IIR register is read, or the interrupt is cleared when the next data is written to the THR register. If only one byte is written to the THR register, CH432 will soon generate a request of "transmit hold register (THR) empty interrupt" as the byte is quickly transferred to the transmit shift register (TSR) to start transmitting. At this point, the next data ready to be transmitted can be written. After all the data in TSR is removed, UART transmission is completed, and the TEMT bit of LSR changes to 1 and is active.

When the MCU receives the THR empty interrupt from UART, if FIFO is enabled, up to 16 bytes can be written to the THR register and FIFO at a time, and the bytes are transmitted automatically by CH432 in sequence. If FIFO is disabled, only one byte can be written at a time. If no data needs to be transmitted, simply exit (the interrupts have been automatically cleared when IIR is read earlier).

In the query mode, the MCU can judge whether the transmit FIFO is empty according to the THRE bit of the LSR register. If THRE is 1, data can be written to THR and FIFO. If FIFO is enabled, it can write up to 16 bytes at a time.

The UART receive data available interrupt (the lower 4 bits of IIR are 04H) means that the number of existing data bytes in the receive FIFO has reached or exceeded the FIFO trigger points selected by RECVTG1 and RECVTG0 of FCR. The interrupt is cleared when reading data from RBR causes the number of bytes in the FIFO below the FIFO trigger points. UART receive data timeout interrupt (the lower 4 bits of IIR are 0CH) means that there is at least one byte of data in the receive FIFO, and it has waited for the time equivalent to the time for receiving 4 data when UART receives data last time and the MCU takes the data last time. The interrupt is cleared when a new data is received again, or the interrupt can also be cleared when the MCU reads RBR once. When the receive FIFO is empty, the DATARDY bit of LSR is 0. When there is data in the receive FIFO, DATARDY bit is 1 and valid.

When the MCU receives the UART receive data timeout interrupt, it can first read one byte from RBR, and then query the DATARDY bit of LSR. If the DATARDY bit is valid, another byte is read until the DATARDY bit is invalid.

When the MCU receives the UART receive data available interrupt, first read the number of bytes set by RECVTG1 and RECVTG0 of RBR, and then query the DATARDY bit of LSR. If the DATARDY bit is valid, read one byte again until the DATARDY bit is invalid, or read all bytes after querying that the DATARDY bit of LSR is valid.

In the query mode, the MCU can judge whether the receive FIFO is empty according to the DATARDY bit of LSR. If the DATARDY bit is 1, read a byte of data from RBR and then query the status of the DATARDY bit. If it is valid, read RBR again until DATARDY bit is 0.

Receive line status interrupt (the lower 4 bits of IIR are 06H) means that CH432 detects errors or exceptions in the UART receiving process after the MCU reads LSR last time. When the line status is read from LSR, the interrupt and the status bit in LSR are cleared. The interrupt is logic "OR" for the bit data BREAKINT, FRAMEERR, PARERR and OVERR of LSR.

MODEM input change interrupt (the lower 4 bits of IIR are 00H) means that CH432 detects the change of MODEM input signal after the MCU reads MSR last time. When MODEM status is read from MSR, the interrupt and the status bit in MSR are cleared. The interrupt is logic "OR" for the bit data △DCD, △RI, △DSR and △CTS of MSR.

7.3. Hardware flow control

Hardware flow control includes automatic CTS (AFE of MCR is 1) and automatic RTS (AFE and RTS of MCR are 1).

If automatic CTS is enabled, CTS pin must be valid before UART sends data. UART transmitter detects CTS pin before sending the next data. When CTS pin is valid, the transmitter sends the next data. In order to stop the transmitter sending the later data, CTS pin must be disabled before the middle of the last stop bit currently sent. The automatic CTS function reduces the interrupt applied to the MCU system. When hardware flow control is enabled, a change in CTS pin level does not trigger a MODEM interrupt as CH432 automatically controls the transmitter based on CTS pin status.

If automatic RTS is enabled, RTS pin output is valid only when there is enough space in FIFO to receive data, and RTS pin output is disabled when the receive FIFO is full. RTS pin output is valid if all data in the receive FIFO is taken or cleared. When the trigger points for the receive FIFO are reached (the number of existing bytes in the receive FIFO is not less than the number of bytes set by RECVTG1 and RECVTG0 of FCR), RTS pin output is invalid, and the transmitter of the other side is allowed to send another data after RTS pin is invalid. Once the data in the receive FIFO is emptied, RTS pin will be automatically re-enabled, so that the transmitter of the other side restores sending.

If both automatic CTS and automatic RTS are enabled (both AFE and RTS of MCR are 1), one side will not send data unless there is sufficient space in the receive FIFO of the other side when RTS pin of one side is

connected to CTS pin of the other side. Therefore, the hardware flow control of CH432 can avoid FIFO overflow and timeout errors during UART reception.

7.4. Parallel interface

The parallel port signal line includes: 8-bit bidirectional data buses D7-D0, read strobe input pin RD#, write strobe input pin WR#, chip select input pins CS# and CS1 as well as address input pins A3-A0 or address latch enable pin ALE. CH432 can be easily hooked to the system buses of various 8-bit DSP and MCU through passive parallel interface, and can coexist with multiple peripheral components.

CS# and CS1 of CH432 are driven by the address decoding circuit, and can be used for device selection when the MCU has multiple peripheral components. When there are fewer peripheral components, the simple chip select and decoding for the addresses can also be performed directly by active low CS# and active high CS1.

For the MCU similar to the Intel parallel port timing, RD# and WR# pins of CH432 can be connected to the read strobe output pin and write strobe output pin of the MCU respectively. For the MCU similar to Motorola parallel port timing, the RD# pin of the CH432 shall be connected to low level, and the WR# pin shall be connected to the read/write direction output pin R/-W of the MCU.

In the direct address mode, the current operation address is input directly by the pins A3-A0 during the access operation.

In the multiplexed address mode, the current operation address is input and latched from the pins D3-D0 during ALE pin high level before the access operation. ALE pin is an alias for the pin A3. When ALE pin is at high level, data appearing on the pins D3-D0 is used as address latch. ALE pin shall be at low level during access operation, so previously latched addresses are not affected.

The following table is the truth table of the parallel port I/O operation (X in the table means that this bit is not concerned, and Z means that three states of CH432 are disabled).

CS1	CS#	WR#	RD#	D7-D0	Actual operation on CH432
0	X	X	X	X/Z	CH432 is not selected, and no any operation
X	1	X	X	X/Z	CH432 is not selected, and no any operation
1	0	1	1	X/Z	Although selected but no operation, no any operation
1	0	0	X	Input	Write data to the specified address of CH432
1	0	1	0	Output	Read data from the specified address of CH432

7.5. SPI

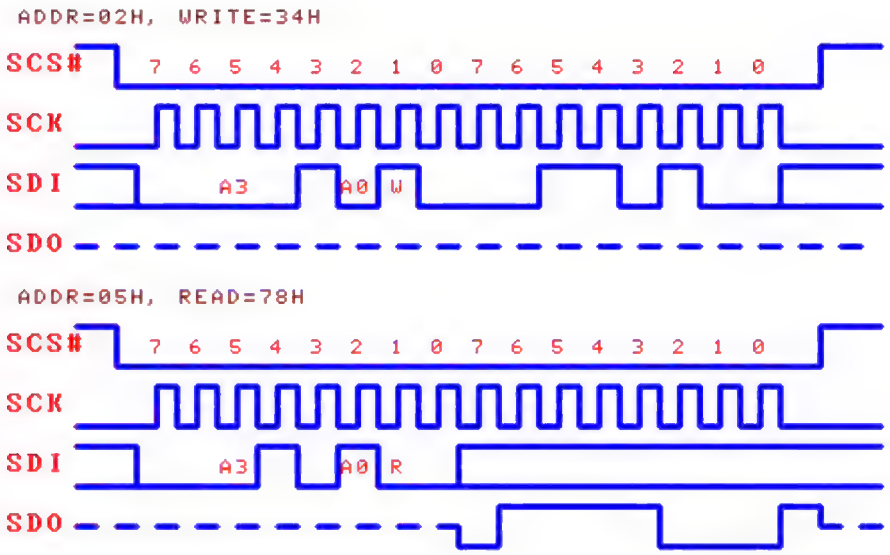
The SPI signal lines include: SPI chip select input pin SCS#, serial clock input pin SCK, serial data input pin SDI and serial data output pin SDO. CH432 can be hooked to SPI serial buses of various DSP and MCU with fewer connections through SPI serial interface by using less connecting wires, or be connected point-to-point over a longer distance.

The SCS# pin of the CH432 is driven by the SPI chip select output pin or the general output pin of the MCU. The SCK pin is driven by the SPI clock output pin SCK of the MCU. The SDI pin is driven by the SPI data output pin SDO or MOSI, and SDO pin is connected to the SPI data input pin SDI or MISO of the MCU. For the hardware SPI interface, it is recommended to set SPI as: CPOL=CPHA=0 or CPOL=CPHA=1, and MSB is first.

The SPI interface of CH432 supports the MCU to simulate SPI interface for communication with the common I/O pins. The SDO of CH432 is a three-status output pin, which will only output after receiving a read operation command. To save pins, the SDO pin of CH432 can be connected in parallel with the SDI pin and then connected to the bidirectional I/O pin of the MCU. It is recommended that the SDO pin of CH432

shall be connected to the SDI pin in series through a resistor with a few hundred ohms.

The SPI interface of CH432 supports SPI mode0 and SPI mode3. CH432 always inputs data from the rising edge of the SPI clock SCK, and outputs data from the falling edge of SCK when the output is allowed. MSB is first, and one byte is composed of 8 bits.



The figure above is a SPI logic timing diagram. The first one shows that 34H is written to 02H address, and the second one shows that 78H is read from 05H address.

Steps of SPI operation:

① The MCU generates the SPI chip select of CH432, which is active at low level;

② The MCU sends a byte of address code according to SPI output mode to specify the operation address and the direction of read/write operation. The bit1 indicates the data transmission direction. If it is 1, write operation and go to step ③. If it is 0, read operation and go to step ④. The bit5 to bit2 specify the current operation address.

③ If it is a write operation, the MCU will send a byte of data to be written. CH432 receives and saves it to the specified address, and go to step ⑤;

④ If it is a read operation, CH432 will read a byte of data from the specified address and outputs it. The MCU receives and saves the data, and go to step ⑤;

⑤ The MCU disables the SPI chip select of CH432 to end the current SPI operation.

7.6. Application specifications

The output pins of CH432 are at CMOS level, compatible with TTL level, and the input pins are compatible with CMOS and TTL levels, and can be further converted to RS232 serial port by adding an external RS232 level converter. Any pins of CH432 not used in the actual circuit can be suspended.

When UARTs of CH432 work normally, the clock signal shall be externally provided for XI pin. Generally, the clock signal is generated by the built-in inverter of CH432 through the crystal stable frequency oscillator. To reduce power consumption, if only one serial port is used, the LOWPOWER bit of IER for another serial port can be set to 1, to disable the unused UART. If two UARTs both are temporarily out of use, the SLP bit of IER for UART0 can be set to 1, to disable the clock oscillator. However, when the clock oscillator is enabled again, it is necessary to wait for the start and stabilization time of at least 3 milliseconds before UART operation.

UART pins of CH432 include: data transmission pins and MODEM contact signal pins. Data transmission pins include: TXD pin and RXD pin, at high level by default. The MODEM contact signal pins include: CTS pin, DSR pin, RI pin, DCD pin, DTR pin and RTS pin, all of which are at high level by default. All these

MODEM contact signals can be used as general-purpose IO pins, controlled by the MCU application program and their purposes can be defined.

CH432 has built-in independent transceiver buffer and FIFO, and supports simplex, half-duplex and full-duplex asynchronous serial communication. Serial data includes 1 low-level start bit, 8 data bits, 0/1 additional verification bit or flag bit, 1/2 high-level stop bits, and supports odd/even/mark/blank verification. CH432 supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M, etc. The baud rate error of UART transmit signal is less than 0.2%, and the allowable baud rate error of UART receive signal is not less than 2%.

CH432 can be used to extend additional high-speed RS232 serial ports through parallel ports or SPI interface for the MCU/embedded system, high baud rate serial ports that support automatic hardware rate control, RS422 and RS485 communication interfaces, SIR infrared communication port, etc. Existing serial port programs developed on the basis of industry standard 16C450 and 16C550 chips can be applied directly without any modification.

8. Parameters

8.1. Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description		Min.	Max.	Unit
TA	Operating ambient temperature	VCC=5V	-40	85	℃
		VCC=3.3V	-40	65	
TS	Storage ambient temperature		-55	125	℃
VCC	Supply voltage (VCC is connected to power, GND to ground)		-0.5	6.0	V
VIO	Voltage on input/output pins		-0.5	VCC+0.5	V

8.2. Electrical characteristics

Test conditions: TA=25℃, VCC=5V

(If the supply voltage is 3.3V, all current parameters in the table need to be multiplied by a factor of 40%)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	3.3	5	5.3	V
ICC	Supply current at 5V	2	5	10	mA
ICC3	Supply current at 3.3V	0.5	1.5	4	mA
ISLP3	Supply current at 3.3V in low-power sleep mode	50	400	600	uA
VIL	Low level input voltage	-0.5		0.8	V
VIH	High level input voltage	2.0		VCC+0.5	V
VOL	Low level output voltage (I_{IL}=4mA)			0.5	V
VOH	High level output voltage (I_{OH}=2mA)	VCC-0.5			V
IIN	The input current without pull-up resistor			10	uA
IUP1	The input current with weak pull-up resistor	2	5	170	uA
VR	Voltage threshold of internal power on reset	2.4	2.7	3.0	V

8.3. Basic timing

Test Conditions: TA=25℃, VCC=5V.

When VCC=3.3V, see values in brackets. Refer to the attached figure.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
FXI	XI input frequency, crystal frequency	0.9216	22.1184	32 (24)	MHz
TPR	Internal reset time when power-on	0.1	1	20	mS
TIC	Time from receiving clear interrupt operation to undoing interrupt	2	20	100	nS

8.4. Parallel port timing

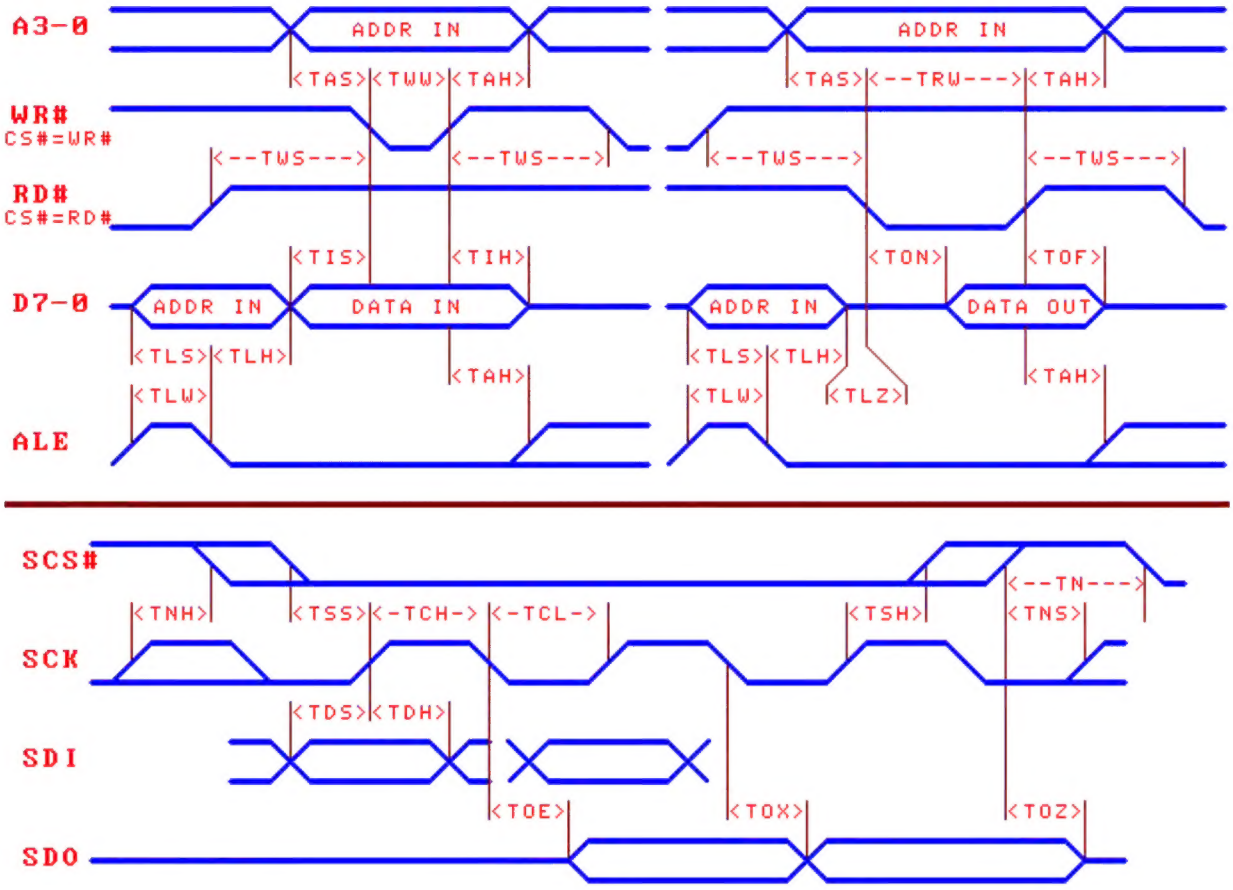
Test conditions: TA=25℃, VCC=5V.

When VCC=3.3V, see values in brackets. Refer to the attached figure.

(RD means that RD# signal is active and CS# signal is active, WR#=1&RD#=CS#=0&CS1=1, perform read operation)

(WR means that WR# signal is active and CS# signal is active, WR#=CS#=0&CS1=1, perform write operation)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
TWW	Write pulse width	40 (60)			nS
TRW	Read pulse width	40 (60)			nS
TWS	Interval width between read strobe pulse or write strobe pulse	60 (90)			nS
TAS	Address input setup time before RD or WR	5 (8)			nS
TAH	Address input hold time after RD or WR	3			nS
TIS	Data input setup time before WR	0			nS
TIH	Data input hold time after WR	3			nS
TON	Read HIGH to data output valid		18 (30)	25 (40)	nS
TOF	Read LOW to data output invalid			20 (35)	nS
TLW	Width of effective address latch pulse ALE	6 (9)			nS
TLS	Address input setup time before address latch ALE	5 (8)			nS
TLH	Address input hold time after address latch ALE	3			nS
TLZ	Multiplexed address output invalid to read HIGH	0			nS



8.5. SPI timing

Test conditions: TA=25°C, VCC=5V.

When VCC=3.3V, see values in brackets. Refer to the attached figure above)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
TSS	SCS# active setup time before SCK rising edge	20 (30)			nS
TSH	SCS# active hold time after SCK rising edge	20 (30)			nS
TNS	SCS# inactive setup time before SCK rising edge	20 (30)			nS
TNH	SCS# inactive hold time after SCK rising edge	20 (30)			nS
TN	SCS# inactive time (SPI operation interval time)	80 (100)			nS
TCH	SCK clock high-level time	20 (30)			nS
TCL	SCK clock low-level time	20 (30)			nS
TDS	SDI input setup time before SCK rising edge	10 (15)			nS
TDH	SDI input hold time after SCK rising edge	5			nS
TOE	SCK falling edge to SDO output active	2	12 (20)	20 (30)	nS
TOX	SCK falling edge to SDO output change		8 (12)	12 (20)	nS
TOZ	SCS# inactive to SDO output inactive			20 (30)	nS

9. Applications

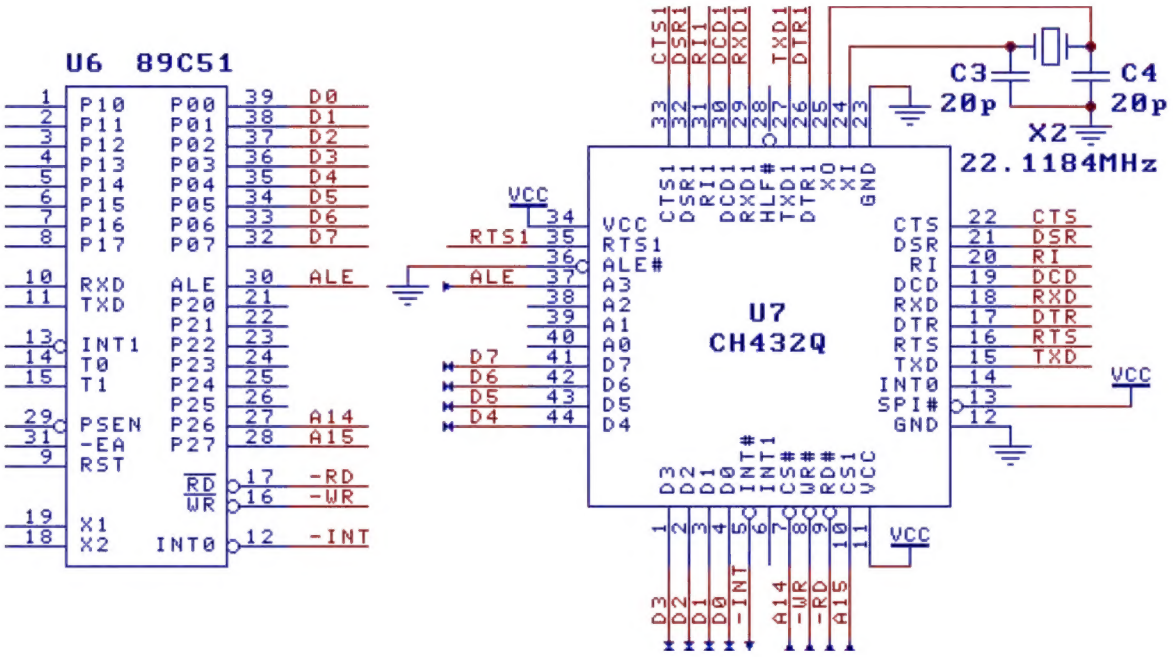
9.1. Parallel multiplexed address mode (Figure below)

This is a double-channel asynchronous serial interface circuit based on CH432Q. The interface mode of CH432 and MCU is the multiplexed address 8-bit parallel port mode. ALE pin is used to input the latch enable signal of multiplexed address, the chip select signals CS1 and CS# are directly driven by the address signal of the MCU, and simple address decoding is performed inside CH432. The chip select address of CH432 is 8000H to 0BFFFH in the figure.

Two UARTs of CH432 in the figure share the INT# interrupt output pin. If it is required to make the interrupts of the two UARTs completely independent, the MCU can be connected to the INT0 pin and the INT1 pin of CH432 (these two interrupt outputs are active at high level and can be used for query).

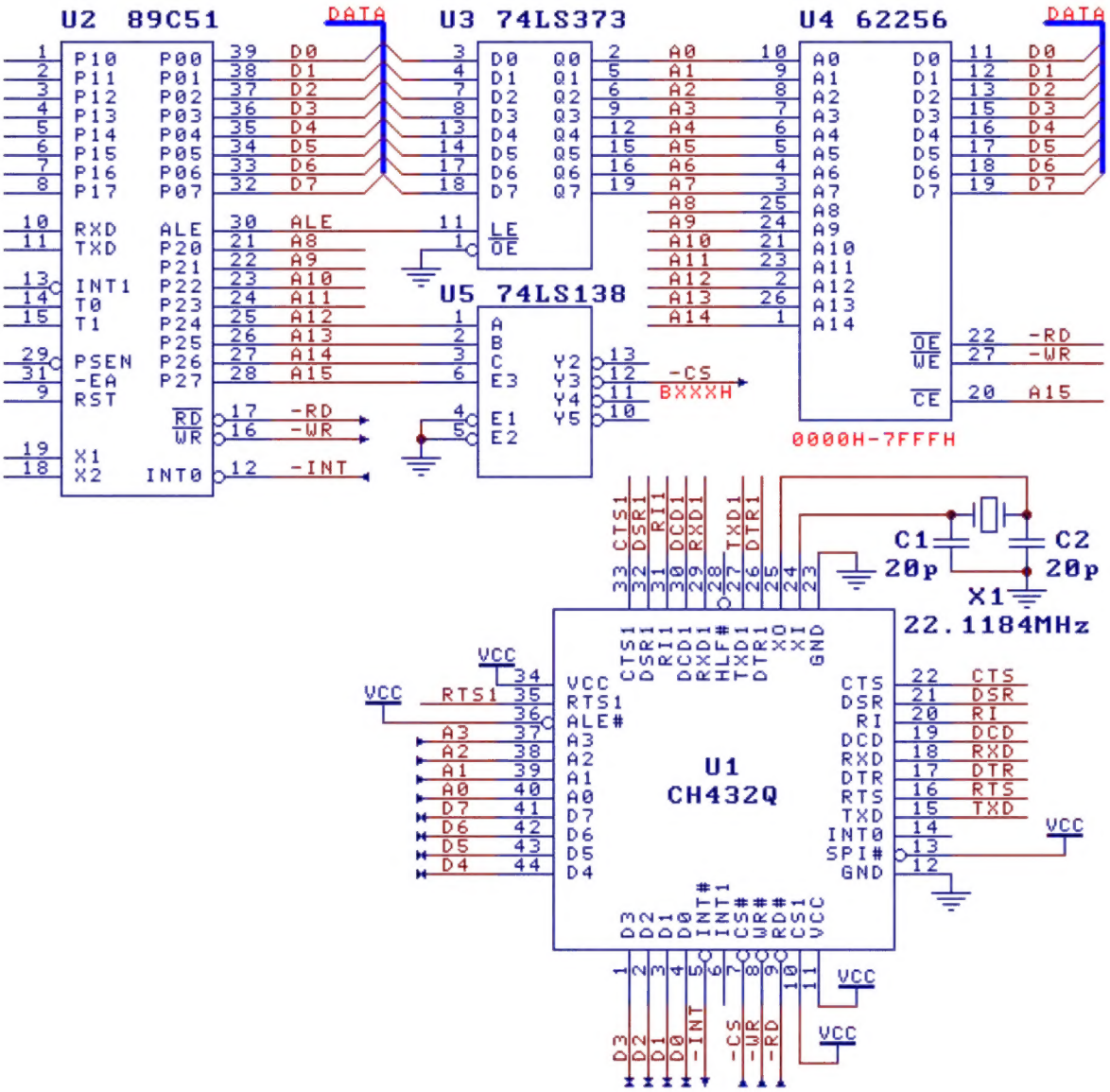
The crystal X2 and the capacitors C3 and C4 are used in the clock oscillation circuit. The frequency of X2 can be selected according to the maximum communication baud rate actually required. In order to reduce power consumption and electromagnetic radiation, it is recommended to select a lower frequency for the crystal X2, such as 7.3728MHz crystal.

The UART and MODEM signals of CH432 are at CMOS/TTL level, and double RS232 serial ports can be realized by adding 75232/MAX213/ADM213/SP213 and other RS232 level converters externally.

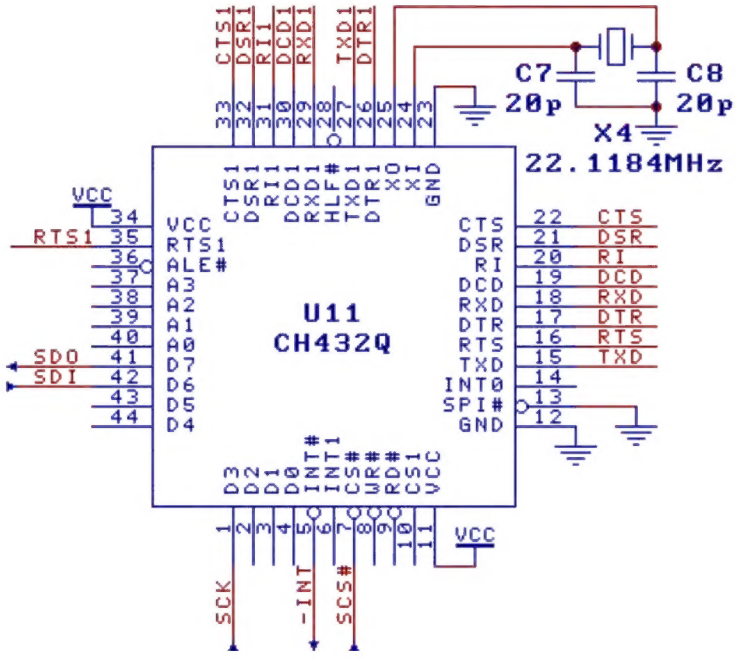


9.2. Parallel direct address mode (Figure below)

In the figure, the interface mode between CH432Q and the MCU is the direct address 8-bit parallel port. ALE# pin is connected to high level, the pins A3-A0 are used to input the direct address, and the chip select signal CS# is driven by the output signal of address decoder U5.



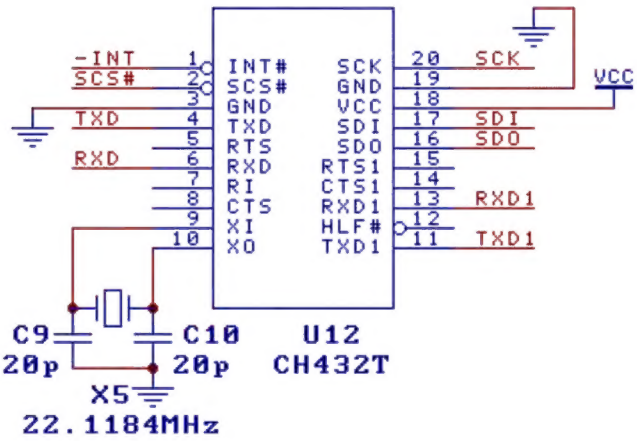
9.3. Complete serial port in SPI mode (Figure below)



This is a double-channel asynchronous serial interface circuit based on CH432Q SPI interface mode. SPI# pin is connected to low level in the figure.

9.4. Simplified serial port in SPI mode (Figure below)

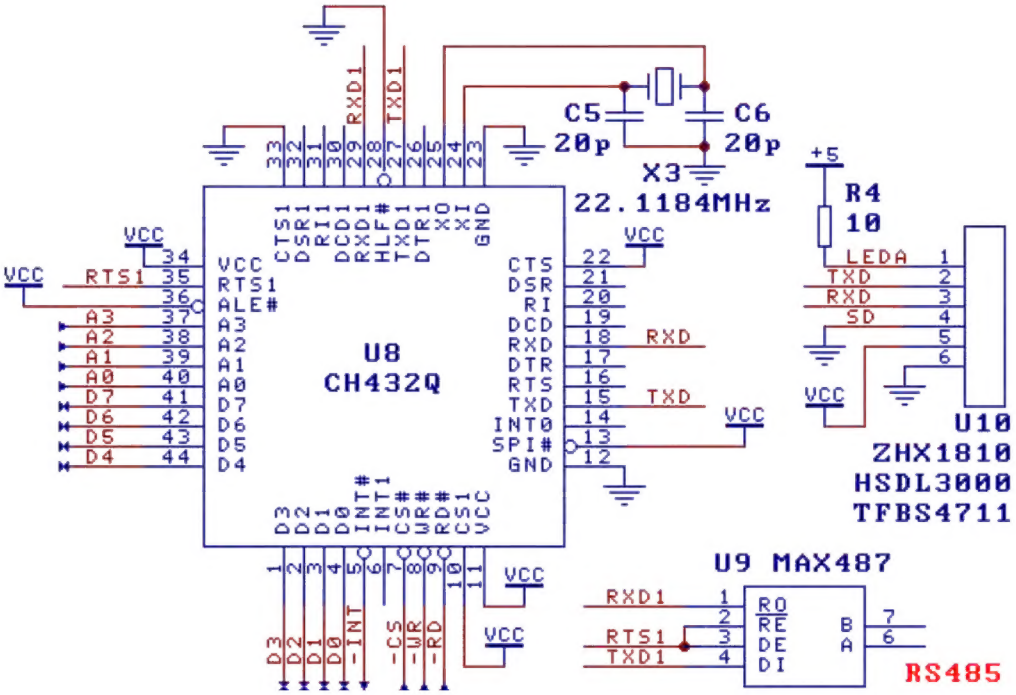
This is a double serial port circuit based on CH432T, with some uncommon MODEM signals removed. Other functions and use methods are the same as that of CH432Q in SPI interface mode.



9.5. RS485 and IrDA application (Figure below)

In the figure, HLF# pin of CH432 is connected to low level, and half-duplex communication mode is selected.

CTS pin of UART0 is at high level. IrDA infrared code/decode mode is selected. It is used for SIR infrared communication through the external infrared transceiver U10.

CTS1 pin of UART1 is at low level. The half-duplex mode is selected. It is used for RS485 communication through the RS485 transceiver U9.

In the half-duplex communication mode, RTS and RTS1 pins indicate the status of serial data being sent, active at high level, and it can be used for automatic receive/transmit switch of RS485 and other half-duplex communications.